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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/786,110	02/26/2004	Akihisa Hongo	2004_0291	1846

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EXAMINER	
WILKINS III, HARRY D	
ART UNIT	**PAPER NUMBER**
1742	

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,110	HONGO ET AL.	
	Examiner	Art Unit	
	Harry D. Wilkins, III	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4,6,8,9,11-13 and 16-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4,6,8,9,11-13 and 16-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/154,895.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status

1. The rejection under 35 USC 102 based on Oka et al has been withdrawn in view of the cancellation of claim 1.

2. The obviousness-type double patenting rejections based on US 6,929,722 and US 6,294,059 have been withdrawn in view of the cancellation of claim 1 and that the claims of the '722 and the '059 patents do not teach or suggest the cleaning unit with a sponge layer as claimed.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2, 4, 6, 17, 20, 21, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 4,774,101) in view of Giles et al (US 4,924,890) and Yoshizawa (US 4,694,527).

Harris et al teach (see figure 1 and abstract) a substrate plating apparatus for electrolessly plating a surface of a semiconductor substrate with metal which included a plating area including at least one plating chamber for containing a plating solution for electrolessly plating a semiconductor substrate with metal, a concentration analyzing device to analyze concentrations of components of the plating solution and a plating

solution preparing device to prepare the plating solution based on the concentration as analyzed by said concentration analyzing device.

Thus, Harris et al fail to teach a cleaning and drying area as claimed, a partition as claimed and that the pressure in the cleaning and drying area was higher than in the plating area.

Giles et al teach (see figures and abstract) a cleaning and drying area for cleaning and drying of processed semiconductor wafers. Giles et al teach (see col. 9, lines 3-25) the concept of applying a higher pressure at "downstream" processing chamber to prevent "upstream" contaminants from flowing forward with the cleaned wafers.

Yoshizawa et al teach (see figures and abstract) a cleaning and drying area for cleaning and drying of processed semiconductor wafers. Giles et al teach (see col. 4, lines 29-43) the concept of applying a higher pressure at "downstream" processing chamber to prevent "upstream" contaminants from flowing forward with the cleaned wafers. Yoshizawa et al further teach (see col. 2) utilizing scrubbing pads (i.e.-a cleaner with a sponge layer) for cleaning a semiconductor wafer.

Therefore, it would have been obvious to one of ordinary skill in the art to have added a cleaning and drying area for cleaning and drying the plated semiconductor wafer because the cleaning and drying area of either Giles et al or Yoshizawa would have removed any contaminants from the surface of the plated semiconductor wafer thereby reducing unsatisfactory wafers. Giles et al and Yoshizawa teach using a higher pressure in a downstream processing location to prevent contamination. Thus, it would

have been obvious to one of ordinary skill in the art to have kept the cleaning and drying area at a higher pressure than the plating area to prevent contaminants entering the cleaning and drying area from the plating area. Both Giles et al and Yoshizawa teach using a partition to allow the differences in pressures between adjacent processing areas.

Regarding claim 4, the concentration analyzing device of Harris et al included (see abstract) a metal ion concentration analyzer and a plating additive concentration analyzer.

Regarding claims 6 and 17, it would have been obvious to one of ordinary skill in the art to have combined the electroless plating chamber of Harris et al with the cleaning and drying station of Giles et al into a single device. A loading and unloading section would have been utilized to load and unload the semiconductor wafers from the device, and it would have been within the ability of one of ordinary skill in the art to have arranged the cleaning and drying area between the loading and unloading station and the plating station because that would prevent contaminants from the plating area from reaching the exterior clean room environment.

Regarding claims 20, 21, 25 and 26, Giles et al teach (see figure 1 and related description) providing clean air to a section by flowing air downward into the processing section. This is done to force any contaminants away from semiconductor wafers. Therefore, it would have been obvious to have the air flow downwardly in both the plating area and the cleaning and drying area to force contaminants away from the semiconductor wafers.

5. Claims 8, 19 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 4,774,101) in view of Giles et al (US 4,924,890) and Yoshizawa (US 4,694,527) as applied to claim 2, 4 and 6 above, and further in view of Dubin et al (US 5,891,513).

It was known in the art at the time of invention that it was conventional to utilize a CMP device after electroless plating in order to remove any excess plated copper. See Dubin et al in the abstract.

Therefore, it would have been obvious to one of ordinary skill in the art to have added a CMP device to the apparatus in order to remove any excess plated copper from the semiconductor wafer.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 4,774,101) in view of Giles et al (US 4,924,890) and Yoshizawa (US 4,694,527) and Dubin et al (US 5,891,513) as applied to claim 8 above, and further in view of Yates (US 4,609,565).

It was known in the art at the time of invention that it was conventional to utilize a pretreatment device before electroless plating in order to enhance the electroless plating of metal. Without the activation step, the metal layer would not stick to the underlying semiconductor material. See Yates at col. 4, lines 23-39).

Therefore, it would have been obvious to one of ordinary skill in the art to have added a pretreatment chamber to the apparatus in order to pretreat the semiconductor wafer for subsequent electroless plating.

7. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 4,774,101) in view of Giles et al (US 4,924,890) and Yoshizawa (US 4,694,527), Dubin et al (US 5,891,513) and Yates (US 4,609,565) as applied to claim 9 above, and further in view of Ishi et al (US 5,806,137).

Yoshizawa does not teach that the scrub pads for scrubbing the surface of the semiconductor wafer were in the shape of a pencil or a roller.

Ishi et al shows (see abstract and figures 1-4) a conventional shape of pads for scrubbing the surface of a semiconductor wafer. The scrubbing pads were in the shape of rollers.

However, both shapes of the scrubbing pads (the rollers of Ishi et al and the flat pads of Yoshizawa) are considered to be functionally equivalent because both were recognized in the art of semiconductor cleaning as being suitable for performing a double-sided cleaning of a semiconductor wafer.

Therefore, it would have been obvious to one of ordinary skill in the art to have substituted the roller scrubbing pads of Ishi et al for the flat scrubbing pads of Yoshizawa because the different shapes of scrubbing pads were art recognized to be functionally equivalent.

Regarding claims 12 and 13, Giles et al teach (see figure 1 and related description) providing clean air to a section by flowing air downward into the processing section. This is done to force any contaminants away from semiconductor wafers. Therefore, it would have been obvious to have the air flow downwardly in both the

plating area and the cleaning and drying area to force contaminants away from the semiconductor wafers.

8. Claims 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 4,774,101) in view of Giles et al (US 4,924,890) and Yoshizawa (US 4,694,527) as applied to claims 2 and 4 above, and further in view of Yates (US 4,609,565).

It was known in the art at the time of invention that it was conventional to utilize a pretreatment device before electroless plating in order to enhance the electroless plating of metal. Without the activation step, the metal layer would not stick to the underlying semiconductor material. See Yates at col. 4, lines 23-39).

Therefore, it would have been obvious to one of ordinary skill in the art to have added a pretreatment chamber to the apparatus in order to pretreat the semiconductor wafer for subsequent electroless plating.

9. Claims 18 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 4,774,101) in view of Giles et al (US 4,924,890) and Yoshizawa (US 4,694,527) as applied to claim 2 and 4 above, and further in view of Ishi et al (US 5,806,137).

Yoshizawa does not teach that the scrub pads for scrubbing the surface of the semiconductor wafer were in the shape of a pencil or a roller.

Ishi et al shows (see abstract and figures 1-4) a conventional shape of pads for scrubbing the surface of a semiconductor wafer. The scrubbing pads were in the shape of rollers.

However, both shapes of the scrubbing pads (the rollers of Ishi et al and the flat pads of Yoshizawa) are considered to be functionally equivalent because both were recognized in the art of semiconductor cleaning as being suitable for performing a double-sided cleaning of a semiconductor wafer.

Therefore, it would have been obvious to one of ordinary skill in the art to have substituted the roller scrubbing pads of Ishi et al for the flat scrubbing pads of Yoshizawa because the different shapes of scrubbing pads were art recognized to be functionally equivalent.

10. Claims 2, 4, 6, 17, 18, 20, 21, 23, 25 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 4,774,101) in view of Nishi et al (US 5,679,059).

Harris et al teach (see figure 1 and abstract) a substrate plating apparatus for electrolessly plating a surface of a semiconductor substrate with metal which included a plating area including at least one plating chamber for containing a plating solution for electrolessly plating a semiconductor substrate with metal, a concentration analyzing device to analyze concentrations of components of the plating solution and a plating solution preparing device to prepare the plating solution based on the concentration as analyzed by said concentration analyzing device.

Thus, Harris et al fail to teach a cleaning and drying area as claimed, a partition as claimed and that the pressure in the cleaning and drying area was higher than in the plating area.

Nishi et al teach (see abstract, figures and col. 7, lines 4-14) a device including a processing area and a cleaning and drying area separated by a partition, where the pressure is maintained at a higher amount in the cleaning and drying area than in the processing area to prevent contaminants from the processing area from entering the cleaning and drying area. The cleaning and drying area of Nishi et al included a cleaning unit comprising a cleaner with a sponge layer (roller 33, see figure 2).

Therefore, it would have been obvious to one of ordinary skill in the art to have added a cleaning and drying area as taught by Nishi et al for cleaning and drying the plated semiconductor wafer because the cleaning and drying area of would have removed any contaminants from the surface of the plated semiconductor wafer thereby reducing unsatisfactory wafers. Nishi et al teach using a higher pressure in the cleaning and drying area to prevent contamination form the processing area. Thus, it would have been obvious to one of ordinary skill in the art to have kept the cleaning and drying area at a higher pressure than the plating area to prevent contaminants entering the cleaning and drying area from the plating area. Nishi et al teach using a partition wall to prevent cross contamination.

Regarding claim 4, the concentration analyzing device of Harris et al included (see abstract) a metal ion concentration analyzer and a plating additive concentration analyzer.

Regarding claims 6 and 17, it would have been obvious to one of ordinary skill in the art to have utilized the electroless plating area of Harris et al as the processing area of Nishi et al because the cleaning and drying area of Nishi et al would have

advantageously reduced unsatisfactory wafers due to contaminants. Nishi et al teach (see figures 3-8) an embodiment where there was a loading and unloading area and the apparatus was arranged such that the cleaning and drying area was between the loading and unloading area and the processing area. Therefore, it would have been obvious to one of ordinary skill in the art to have similarly arranged the combination of Harris et al and Nishi et al to achieve various advantages, discussed in cols. 7-10, including simple design and prevention of counterflow of air.

Regarding claims 20, 21, 25 and 26, Nishi et al teach exhaust ports located at the lower portions of the different areas, thereby generating a downward flow of air.

Regarding claims 18 and 23, Nishi et al teach using (see figure 2) utilizing a roller shaped cleaner.

11. Claims 8, 19 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 4,774,101) in view of Nishi et al (US 5,679,059) as applied to claim 2, 4 and 6 above, and further in view of Dubin et al (US 5,891,513).

It was known in the art at the time of invention that it was conventional to utilize a CMP device after electroless plating in order to remove any excess plated copper. See Dubin et al in the abstract.

Therefore, it would have been obvious to one of ordinary skill in the art to have added a CMP device to the apparatus in order to remove any excess plated copper from the semiconductor wafer.

12. Claims 9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 4,774,101) in view of Nishi et al (US 5,679,059) and Dubin et al

(US 5,891,513) as applied to claim 8 above, and further in view of Yates (US 4,609,565).

It was known in the art at the time of invention that it was conventional to utilize a pretreatment device before electroless plating in order to enhance the electroless plating of metal. Without the activation step, the metal layer would not stick to the underlying semiconductor material. See Yates at col. 4, lines 23-39).

Therefore, it would have been obvious to one of ordinary skill in the art to have added a pretreatment chamber to the apparatus in order to pretreat the semiconductor wafer for subsequent electroless plating.

Regarding claim 11, Nishi et al teach using (see figure 2) utilizing a roller shaped cleaner.

Regarding claims 12 and 13, Nishi et al teach exhaust ports located at the lower portions of the different areas, thereby generating a downward flow of air.

13. Claims 16 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al (US 4,774,101) in view of G Nishi et al (US 5,679,059) as applied to claims 2 and 4 above, and further in view of Yates (US 4,609,565).

It was known in the art at the time of invention that it was conventional to utilize a pretreatment device before electroless plating in order to enhance the electroless plating of metal. Without the activation step, the metal layer would not stick to the underlying semiconductor material. See Yates at col. 4, lines 23-39).

Therefore, it would have been obvious to one of ordinary skill in the art to have added a pretreatment chamber to the apparatus in order to pretreat the semiconductor wafer for subsequent electroless plating.

Response to Arguments

14. Applicant's arguments with respect to claims 2, 4, 6, 8, 9, 11-13 and 16-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Harry D. Wilkins, III whose telephone number is 571-272-1251. The examiner can normally be reached on M-F 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy V. King can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

hdw

HARRY D. WILKINS, III
PRIMARY EXAMINER